WHAT IS CLAIMED IS:

1. A pulse width modulation amplifier which supplies to a load circuit an amplified output having been subjected to a pulse width modulation, comprising:

a first series circuit including a first switching element connected to a positive pole side of a first direct-current power source, and a second switching element, one end of said load circuit being connected to a connecting point between said first switching element and said second switching element,

a second series circuit including a third switching element connected to a positive pole side of a second direct-current power source, and a fourth switching element, the other end of said load circuit being connected to a connecting point between said third switching element and said fourth switching element, and

a driving circuit which turns on a set of said first switching element and said fourth switching element, and a set of said second switching element and said third switching element, set-by-set, each of said sets being alternately put into on-state.

2. A pulse width modulation amplifier which supplies to a load circuit an amplified output having been subjected to a pulse width modulation, comprising:

a first bridge circuit having a series circuit connecting the first switching element and the second switching element, and a series circuit connecting the third switching element being connected to said first switching element, and the fourth switching element, a connecting point between said first and said third switching element being connected to a first direct-current power source, and a connecting point between said first and said second switching elements being connected to a connecting point between said third and said fourth switching element by way of said load circuit,

a second bridge circuit having a series circuit connecting the fifth switching element and the sixth switching element, and a series circuit connecting the seventh switching element being connected to said fifth switching element, and the eighth switching element, a connecting point between said fifth and said seventh switching elements being connected to a second direct-current power source, and a connecting point between said fifth and said sixth switching elements being connected to a

connecting point between said seventh and said eighth switching element by way of said load circuit, and

a driving circuit which turns on a first set of said first and fourth switching elements,

a second set of said second and third switching elements, a third set of said fifth and eighth switching elements and

a fourth set of said sixth and seventh switching elements set-by-set, so that said first set and said third set being alternately turned on, and between the periods when said first set and said third are in on-state, an ON period of said second set and an ON period of said fourth set alternately existing.